Amendments to the Claims

Claims 1-47 (Canceled).

48. (Original): A method of forming an electronic component comprising:

forming first and second conductive materials over a substrate, the second material having a higher oxidation rate than an oxidation rate of the first material when exposed to a thermal oxidizing atmosphere;

first etching the first and second conductive materials to form a conductive component, the conductive component having opposing outer lateral edges of the first and second conductive materials which span between the opposing outer lateral edges;

second etching into both of the second material outer lateral edges to recess them inside of the first material outer lateral edges; and

after the second etching, exposing the substrate to the thermal oxidizing atmosphere effective to grow an oxide layer over both of the outer lateral edges of the first and second conductive materials.

49. (Original): The method of claim 48 wherein one of the first and second conductive materials comprises conductively doped semiconductive material and the other comprises a refractory metal.

50. (Original): The method of claim 49 wherein the refractory metal is in silicide form.

51. (Original): The method of claim 48 wherein the second etching comprises wet etching.

52. (Original): The method of claim 48 wherein the first etching comprises dry etching and the second etching comprises wet etching.

53. (Original): The method of claim 48 wherein the second etching comprises wet etching with a basic solution.

54. (Original): The method of claim 48 wherein the second etching comprises wet etching with a solution comprising ammonium hydroxide and hydrogen peroxide.

55. (Original): The method of claim 48 comprising forming the second conductive material to be received over the first conductive material.

56. (Original): The method of claim 48 wherein the first etching is conducted to space the opposing linear outer lateral edges less than 1 micron apart from one another.

57. (Original): The method of claim 48 comprising forming a third insulative material over the first and second conductive materials, the first etching also etching the third insulative material to form the conductive component to have an insulative cap, the third insulative material having a lower oxidation rate than the second conductive material when exposed to the oxidizing atmosphere, the second etching recessing the second material outer lateral edges to within outer lateral edges of the third insulative material.

58. (Original): The method of claim 48 wherein the electronic component is a conductive line.

59. (Original): The method of claim 58 wherein the conductive line is field effect transistor gate line.

60. (Original): A method of forming an electronic component comprising:

forming first and second conductive materials over a substrate, the second material having a higher oxidation rate than an oxidation rate of the first material when exposed to a thermal oxidizing atmosphere;

first etching the first and second conductive materials to form a conductive component, the conductive component having at least one outer lateral edge of the first and second conductive materials;

second etching into the at least one second material outer lateral edge to recess it inside of the first material outer lateral edge; and

after the second etching, exposing the substrate to the thermal oxidizing atmosphere effective to grow an oxide layer over the at least one outer lateral edge of the first and second conductive materials.

61. (Original): The method of claim 60 further comprising:

after the exposing, depositing an insulating layer to be received over the grown oxide layer over the at least one opposing outer lateral edge; and

anisotropically etching the insulating layer to form an anisotropically etched spacer received over the grown oxide layer over the at least one opposing outer lateral edge.

62. (Original): The method of claim 60 wherein the exposing is effective to fill the second material recesses formed by the second etching.

63. (Original): The method of claim 60 wherein the at least one outer lateral edge extends entirely through the thicknesses of both the first and second conductive materials.

64. (Original): The method of claim 60 wherein the electronic component is a conductive line.

65. (Original): The method of claim 64 wherein the conductive line is field effect transistor gate line.

66. (Original): A conductive line comprising:

a semiconductive substrate;

a stack comprising a conductive layer over the semiconductive substrate, a second conductive layer different in composition from the first and received over the first, and an insulative cap over the second conductive layer; the first conductive layer of the stack having opposing outer lateral edges which are spaced less than one micron apart defining a conductive line width of less than one micron, the second conductive layer of the stack having opposing outer lateral edges which are recessed laterally within the opposing outer lateral edges of the first conductive layer and which are thereby spaced apart less than the opposing outer lateral edges of the first conductive layer are spaced apart, the insulative cap having opposing outer lateral edges in a final circuit construction of the conductive line, the insulative cap having a topmost surface; and

a continuously extending oxide layer formed over the insulative cap topmost surface and laterally over each of the outer lateral edges of the first conductive layer, over each of the outer lateral edges of the second conductive layer and over each of the outer lateral edges of the insulative cap in the final circuit construction of the transistor; the oxide layer in the final circuit construction of the conductive line having opposing substantially continuous straight linear outermost lateral edges extending laterally along and laterally overlapping with all of each of the opposing outer lateral edges of the insulative

cap and all of each of the opposing outer lateral edges of the second conductive layer.

67. (Original): The conductive line of claim 66 wherein the opposing linear outer lateral edges of the oxide layer are formed to be less than 1 micron apart.

68. (Original): The conductive line of claim 66 wherein the oxide layer has a lateral thickness of less than 100 Angstroms over the first conductive layer.

69. (Original): The conductive line of claim 66 wherein the oxide layer has a lateral thickness of less than 100 Angstroms and greater than 10 Angstroms over the first conductive layer.

70. (Original): The conductive line of claim 66 further comprising an insulative spacer formed laterally over the oxide layer.

71. (Original): The conductive line of claim 66 further comprising an insulative spacer formed laterally over the oxide layer; the insulative spacer extending laterally along portions of each of the insulative cap, the first conductive layer, and the second conductive layer.

72. (Original): The conductive line of claim 66 further comprising an insulative spacer formed laterally over the oxide layer, the insulative spacer being laterally narrower at its topmost portion as compared to its lowestmost portion.

73. (Original): The conductive line of claim 66 further comprising an insulative spacer formed laterally over the oxide layer; the insulative spacer extending laterally along portions of each of the insulative cap, the first conductive layer, and the second conductive layer; and the insulative spacer being laterally narrower at its topmost portion as compared to its lowestmost portion.

74. (New): A method of fabricating a transistor gate comprising:

patterning first and second material layers to form a transistor gate stack, wherein the second material has a higher oxidation rate than an oxidation rate of the first material when exposed to a thermal oxidizing atmosphere; and

exposing vertical surfaces of the patterned first and second material layers to the thermal oxidizing atmosphere to form an insulative layer having substantially continuous straight linear outer lateral edges not containing outward lateral bulges.

75. (New): The method of claim 74 further comprising removing a portion of the patterned second material prior to exposing the vertical surfaces of the patterned first and second material layers to the thermal oxidizing atmosphere.

76. (New): The method of claim 75 further comprising implanting ions to form source and drain regions substantially aligned with the outer lateral edges of the insulative layer.

77. (New): A method of forming a lateral oxide layer on a transistor gate stack comprising:

compensating for different oxidation rates of transistor gate stack materials; and

exposing the transistor gate stack materials to a thermal oxidizing atmosphere to form an insulative layer having substantially continuous straight linear outer lateral edges.

78. (New): The method of claim 77 wherein compensating for different oxidation rates comprises removing a portion of a first gate stack material which has a higher oxidation rate than an oxidation rate of a second gate stack material when exposed to a thermal oxidizing atmosphere.

79. (New): A method of forming a lateral oxide layer on a transistor gate stack comprising:

patterning first and second material layers to form a transistor gate stack having vertically aligned side surfaces, wherein the second material has a higher oxidation rate than an oxidation rate of the first material when exposed to a thermal oxidizing atmosphere;

altering a profile of the vertically aligned side surfaces to compensate for different oxidation rates of the first and second material layers; and

exposing the vertical side surfaces of the first and second material layers to the thermal oxidizing atmosphere to form an insulative layer having substantially continuous straight linear outer lateral edges not containing outward lateral bulges.